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09/735,944	12/14/2000	Menno Spijker	10375-US	8083

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CANADA

EXAMINER	
CHANG, EDITH M	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/735,944	SPIJKER ET AL.	
	Examiner	Art Unit	
	Edith M Chang	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12/14/00 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5,7*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "sampling circuits" cited in claim 24 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 17, 19 and 21 are objected to because of the following informalities:

Claim 17, the term "said clock recovery phase locked loop" is suggested to be changed to "said phase locked loop".

Claim 19, The term "said remote and locally generated time stamps" is suggested to be changed to "said remote time stamp and locally generated time stamp".

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 19-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 19, the "counter receiving the inputs of the respective comparators" is not taught in the drawing (Fig.8) of the specification.

Claim 20, the "an error flag to disable the counter when an error occurs" does not taught in the written description of the specification.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 7 recites the limitation "the weighted output" in "the weighted output is fed to the accumulator". There is insufficient antecedent basis for this limitation in the claim.

Claim 16 provides for the use of a multimode clock recovery circuit cited in claim 1 which is an apparatus claim, but, since the claim does not set forth any steps involved in the method/process, it is unclear what method/process applicant is intending to encompass. A claim is indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

Claim 16 is rejected under 35 U.S.C. 101 because the claimed recitation of a use, without setting forth any steps involved in the process, results in an improper definition of a process, i.e., results in a claim which is not a proper process claim under 35 U.S.C. 101. See for example *Ex parte Dunki*, 153 USPQ 678 (Bd.App. 1967) and *Clinical Products, Ltd.* v. *Brenner*, 255 F. Supp. 131, 149 USPQ 475 (D.D.C. 1966).

Claim 21, recites the limitation "said adder". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-2, 4, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Muntz et al. (US 5896427).

Regarding **claim 1**, Muntz et al. discloses a multimode clock recovery circuit (FIG.7) for providing constant bit rate services in a cell relay network (column 2 lines 44-58), comprising an embedded digital phase locked loop (704-706 FIG.7, wherein the 706 is one of the multimode, 406 FIG.4, 506 FIG.5 or 606 FIG.6) including an input circuit (704 FIG.7) capable of generating a phase signal form at least two types of input signal (716 FIG.7 is the phase signal), the phase

signal controlling the output the phase lock loop to generate clock signals (716-706-324 FIG.7, where 324 are the clock signals).

Regarding **claim 2**, Muntz et al. discloses the input circuit (502 FIG.5) is adapted to receive a phaseword from a receive buffer (FIG.5 520 is the buffer, 570 CURRENT FIFO DEPTH is the phaseword) to permit clock adaptive recovery based on the fill level of the receive buffer for incoming cells.

Regarding **claim 4**, Muntz et al. discloses a phase detector (404 FIG.4) having a first input for receiving a feedback signal (FIG.4 464-436, where 464 is the feedback signal, the receiving input of 426 is the first input), and at least one additional input for receiving either a clock signal or a timestamp signal (432/434 is the one additional input).

Regarding **claim 16**, Muntz et al. discloses the use of the multimode clock recovery circuit to filter an input clock prior to the generation of SRTS timestamps (FIG.4 where the 402 INPUT STAGE filters out an input clock prior to the generation of SRTS timestamps by 426).

8. Claim 19 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Bleiweiss et al. (US 6144714).

Regarding **claim 19**, Bleiweiss et al. discloses a phase detector (FIG.6) for recovering signals from received time stamps in a cell relay network (FIG.4), comprising a first input for receiving a remote time stamp signal (121 FIG.6), a second input for receiving a locally generated time stamp signal (137 FIG.6), comparators for comparing the current time stamps with the previous time stamps (151/153 FIG.6), a weighted up/down counter (155-157-161 FIG.6), a subtractor (155 FIG.6) for deriving the difference of the remote and locally generated

time stamps, and an accumulator (167 FIG.6) for adding the output of the subtractor to the output of the counter.

Regarding **claim 21**, Bleiweiss et al. discloses a register connected to the output of the adder for storing the phase output (167 FIG.6 is the adder, a register connected to the output of the adder to store the result of the adder is part of the structure of the adder).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muntz et al. (US 5896427) as applied to claim 1 above, and further in view of Lien (US 5396492).

Regarding **claim 3**, Muntz et al. does not explicitly specify the phaseword/FIFO level, however Line teaches the phaseword is derived from write_point – read_pointer –average (FIG.1 14 is the write_point, 24 is the read_point, column 2 lines 45-50, lines 55-57, column 5 lines 8-10, where a nominal value is the average that the deviation/error/difference of the actual fill level of FIFO and the average is derived/calculated, FIG.1 29 where the calculation is performed). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the phaseword taught by Lien as the FIFO level of the Muntz et al.'s system to have sufficient gain to meet clock tracking and wander specification (column 2 lines 5-6).

11. Claims 5, 11-13, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muntz et al. (US 5896427) as applied to claim 4 above, and further in view of Bleiweiss et al. (US 6144714).

Regarding **claim 5**, further Bleiweiss et al. teaches a common up/down counter (FIG.6 155-157-161). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the Bleiweiss et al.'s phase detector implemented in Muntz et al.'s timing control stage/phase detector to limit the frequency deviation of the recovered clock (column 10 lines 15-20).

Regarding **claim 11**, Muntz et al. discloses a SRTS generator in the feedback loop of the PLL (436 FIG.4).

Regarding **claim 12**, further Bleiweiss et al. teaches the SRTS generator comprising a divider (131-135 FIG.5) for receiving a feedback signal from the PLL, a counter (139 FIG.5) for receiving the network clock signal (F_{NET} FIG.5), and a register (137 FIG.5) for generating a local SRTS signal. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the Bleiweiss et al.'s phase detector implemented in Muntz et al.'s timing control stage/phase detector to limit the frequency deviation of the recovered clock (column 10 lines 15-20).

Regarding **claim 13**, further Bleiweiss et al. teaches the inputs of the counter (FIG.6 155-157-161 is the counter) receive the respective network clock signal (FIG.6 121) and the local SRTS signal (FIG.6 137).

Regarding **claim 17**, Muntz et al. discloses the output of the PLL (FIG.4 464) is fed to the input of the SRTS generator (FIG.4 436) to dejitter incoming clock signals.

12. Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muntz et al. (US 5896427) as applied to claim 5 above, and further in view of Bleiweiss et al. (US 6144714).

Regarding **claims 6 & 7**, further Bleiweiss et al. teaches the output counter (FIG.6 155-157-161) is fed to an accumulator (FIG.6 167 where the output is weighted by 161 /with out applying a modulo function). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the Bleiweiss et al.'s phase detector implemented in Muntz et al.'s timing control stage/phase detector to limit the frequency deviation of the recovered clock (column 10 lines 15-20).

Regarding **claim 8**, Muntz et al. discloses the output of the phase detector (which includes the counter) can be changed for receiving either a clock signal (432 FIG.4) or a signal form a timestamp circuit (434/444 FIG.4).

Regarding **claim 9**, further Bleiweiss et al. teaches the weight of the counter is programmable (column 9 lines 27-32 where the value, such as sixteen, of weight/G is selected by design options).

Regarding **claim 10**, further Bleiweiss et al. teaches first and second difference circuits (FIG.6 151, 153), each receiving an SRTS input signal and an SRTS input signal delayed by one cell (column 9 lines 10-15 where the current and previous samples are delayed apart by one cell, refer to FIG.2 '427), the first circuit receiving its SRTS from the network (FIG.6 121-151, and the second difference circuit receiving its SRTS signal from a local SRTS generator (FIG.4 137-153), the first difference circuit providing an input to the counter (FIG.6 151 to 155-157-161) and the second difference circuit providing an input to a subtractor (FIG.6 153 to 155), the output of the difference circuit being fed to the accumulator with the weighted output (FIG.6 161-167).

13. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muntz et al. (US 5896427) as applied to claim 1 above, and further in view of Peres et al. (US 6144674).

Regarding **claim 14**, further Peres et al. teaches the holdover mold of the PLL wherein the output of the PLL remains constant based on the last valid input signal when a valid input signal is lost (column 2 lines 5-10). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the holdover taught by Peres et al. in the Muntz et al.'s method when the sources is not available, to keep the output frequency of the PLL fixed and no further corrections needed (column 2 lines 61-65).

Regarding **claim 15**, further Peres et al. teaches that the PLL is placed into holdover when it is switched over to the other sources while it losses the valid signal (Abstract, column 2 lines 5-10). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the holdover taught by Peres et al. in the Muntz et al.'s method when the sources is not available (such as the buffer runs out in SRTS mode, times out in ACR mod, and loss of sync in the SNC mode), to keep the output frequency of the PLL fixed and no further corrections needed (column 2 lines 61-65).

14. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muntz et al. (US 5896427) in view of Brauns (US 5442324) and McCaslin (US 5036294).

Regarding **claim 18**, Mutz et al. discloses a multimode clock recovery circuit including a

phase lock loop (PLL) and an SRTS generator in the feedback loop (436 FIG.4 is the SRTS generator, 460-464-436 is the loop), however does not detail (1) the content structure of the PLL with (2) jitter reduction circuit specified explicitly.

With respect to item (1), Brauns teaches the PLL with the digital controlled oscillator (DCO) in FIG.2 which comprising a phase detector (600 FIG.2) having multiple inputs, a loop filter receiving the output of the phase detector (700 FIGF.2), a DCO receiving the output of the loop filter (800 FIG.2), a divider receiving the output of the DCO. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the PLL with the DCO taught by Brauns in Muntz et al.'s CLOCK GENERATION STAGE to have a cost effective PLL circuitry with the DCO having a smaller phase adjustment (column 1 lines 10-30).

With respect to item (2), McCaslin teaches the jitter reduction circuit (34 FIG.2) in the PLL to receive the output from the oscillator (32 FIG.2, column 3 lines 35-45). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the jitter reduction circuit taught by McCaslin in the Muntz et al.'s CLOCK GENERATION STAGE (with Brauns' detail structure) to receive the output from the DCO/the oscillator, to reduce the intrinsic jitter (Abstract, column 5 lines 25-37).

15. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muntz et al. (US 5896427) in view of Brauns (US 5442324) and McCaslin (US 5036294) as applied to claim 18 above, and further in view of Schultz (US 5561469).

Regarding **claim 20**, further Schultz teaches an error flag to disable the counter when an error occurs (column 10 lines 24-37). At the time of the invention, it would have been obvious to

a person of ordinary skill in the art to have the error flag in the counter taught by Schultz in Muntz et al's phase detector (which includes the counter) to prevent continued counting when the error occurs.

16. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muntz et al. (US 5896427) in view of Peres et al. (US 6144674).

Regarding **claim 22**, except specify the holdover of the PLL, Muntz et al. discloses the method of recovering clock signals in a cell relay network providing constant bit rate services, comprising the steps cited in the claim. However Peres et al. teaches placing the PLL into holdover when it is switched over to the other sources while it losses the valid signal (Abstract, column 2 lines 5-10). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the holdover taught by Peres et al. in the Muntz et al.'s method when the sources is not available (such as the buffer runs out in SRTS mode, times out in ACR mod, and loss of sync in the SNC mode), to keep the output frequency of the PLL fixed and no further corrections needed (column 2 lines 61-65).

17. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muntz et al. (US 5896427) in view of Bleiweiss et al. (US 6144714).

Regarding **claim 23**, except explicitly specify the counter, Muntz et al. discloses the method comprising the steps of detecting the phase difference between the input signal and a feedback signal by feeding the clock signals (404 FIG.4, the 464 is the feedback signal inputting to the 436 of the 404, the 450 is the phase difference between the input signal and the feedback

signal). However Bleiweiss et al. teaches the counter to accumulate the output of the counter to create a phase output signal (FIG.6 157 is the counter, 165 accumulates the output of the counter, up or down, wrap or no-wrap are provide as the characteristics of the counter). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the Bleiweiss et al.'s teaching in Muntz et al.'s timing control stage/phase detector to limit the frequency deviation of the recovered clock (column 10 lines 15-20).

Regarding **claim 24**, Bleiweiss et al. discloses a counter (155-157-161 FIG.6) is switchable between a pair of difference circuits (151, 153 FIG.6) and a pair of sampling circuits (121, 137 FIG.6) to receive SRTS and input clock signals. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the Bleiweiss et al.'s teaching in Muntz et al.'s timing control stage/phase detector to limit the frequency deviation of the recovered clock (column 10 lines 15-20).

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M Chang whose telephone number is 703-305-3416. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
February 6, 2004

CHIEH M. FAN
PRIMARY EXAMINER